CLAIMS

What is claimed is:

We claim:

1. An apparatus, comprising:

a graphics-rendering engine to concurrently render two or more independent images for display on multiple display devices; and

a time allocator to arbitrate the use of the graphics-rendering engine between the two or more independent images.

2. The apparatus of claim 1, wherein the time allocator comprises:

a plurality of registers including a first register, the first register having a plurality of fields including a first field to determine whether the first register participates in an arbitration process to use the graphics rendering engine and a second field to point to a memory location containing instructions from a first instruction stream.

3. The apparatus of claim 2, wherein the time allocator further comprising:

A first module to establish a programmable elapsed period of time to use the graphics-rendering engine.

4. The apparatus of claim 3, wherein the time allocator further comprises:

a first circuit to generate a signal to check if a second register should be allowed to use the graphics-rendering engine after the first register uses the graphics-rendering engine for the programmable elapsed period of time.

5. The apparatus of claim 2, wherein the time allocator further comprises:

a first module to direct the graphics-rendering engine to process instructions associated with a first independent image, the instructions stored in a first memory area, the first memory area having an address defined by information contained within the plurality of the fields.

6. The apparatus of claim 5, wherein the first memory area has a start and an end, the first memory area may wrap-around instructions from the end of the first memory area to the start of the first memory area.

7. The apparatus of claim 5, wherein the first module comprises:

a second circuit to track which register in the plurality of registers is currently being serviced by the graphics-rendering engine; and

a third circuit to manage the use of the graphics-rendering engine between a second register which does not participate in the arbitration process and the first register and a third register which participate in the arbitration process.

8. The apparatus of claim 3, wherein the first module comprises:

a first circuit to track the period of elapsed time that a particular register uses the graphics-rendering engine; and

a second circuit to convert the programmable elapsed period of time into an equivalent number of clock cycles.

9. The apparatus of claim 1, wherein the time allocator comprises;

a first circuit to permit a graphics device instruction from a graphics application to direct the graphics-rendering engine to process instructions associated with a second independent image while waiting for an asynchronous event to occur for a first independent image.

10. The apparatus of claim 1, wherein the time allocator comprises:

a first circuit to implement a software instruction from a graphics application, the software instruction to yield time allotted for instructions associated with a first independent image to use the graphics-rendering engine over to instructions associated with a second independent image.

11. The apparatus of claim 1, further comprising:

a first display device and a second display device.

12. The apparatus of claim 1, further comprising:

a graphics context manager to restore information from a memory to the graphics-rendering engine, the information describing a rendering context associated witha first

independent image to be rendered by the graphics-rendering engine, the first independent image being included in the two or more independent images.

13. The apparatus of claim 1, further comprising:

a first memory area to receive instructions for one or more independent images included in the two or more independent images, and

a second memory area to receive instructions for one or more independent images included in the two or more independent images.

14. The apparatus of claim 1, further comprising;

One or more instruction transports to deliver instructions for the two or more independent images to the graphics-rendering engine, the one or more instruction transports including a first instruction transport.

15. The apparatus of claim 14, wherein each instruction transport is associated with a particular display device.

16. The apparatus of claim 14, wherein the first instruction transport comprises:

an instruction memory area;

a first register to define a start and an end to the instruction memory area; and

a memory access engine to fetch and deliver the instructions from the instruction memory area to the graphics-rendering engine.

17. The apparatus of claim 14, wherein the instruction transport further comprises:

a third memory area to store an independent sequence of instructions that can be invoked from an instruction stream.

18. The apparatus of claim 16, wherein the first register contains a first field to instruct the graphics device to write content contained in a second field to a snooped memory location on a periodic basis in order to automatically report an amount of free space available in the instruction memory area.

19. A method, comprising:

using a single graphics-rendering engine to execute instructions associated with a first instruction-stream;

concurrently rendering a first independent image via instructions associated with the first instruction-stream and a second independent image via instructions associated with a second instruction-stream by using the single graphics-rendering engine; and

arbitrating the use of the single graphics-rendering engine between the instructions associated with the first instruction-stream and the instructions associated with the second instruction-stream.

20. The method of claim 19, further comprising:

allocating the concurrent use of the single graphics-rendering engine between the instructions associated with the first instruction-stream and the instructions associated with the second instruction-stream by using a timing mechanism.

21. The method of claim 19, further comprising:

restoring information from a first memory address to the graphics-rendering engine, the information describing a first rendering context associated with the first independent image to be rendered by the single graphics-rendering engine, and storing the information describing a second rendering context associated with the second independent image to a second memory address, the second independent image being rendered by the single graphics-rendering engine.

22. The method of claim 19, further comprising:

displaying one or more images on the multiple display devices.

23. A method, comprising:

concurrently rendering independent images for display on multiple display devices with a graphics-rendering engine;

allocating time use of the graphics-rendering engine between each independent image being rendered; and

storing in a memory area and restoring from the memory area a first rendering context associated with a first independent image.

24. The method of claim 23, further comprising:

determining whether a first register associated with a first independent image participates in an arbitration process to use the graphics-rendering engine.

25. The method of claim 24, further comprising:

permitting, via a software instruction from a graphics application, the graphics-rendering engine to process instructions associated with a second image while waiting for an asynchronous event to occur to a first image.

26. The method of claim 24, further comprising:

yielding time allotted to use the graphics-rendering engine for instructions associated with the first independent image over to instructions associated with a second independent image via a software instruction from a graphics application.

27. The method of claim 23, further comprising:

defining the memory area by programmable content contained in a first register, the memory area dedicated to storing the instructions associated with a first instruction stream.

28. The method of claim 23, further comprising:

establishing a time unit quanta in the timing circuit compatible with a first device operating at a first core frequency and compatible with a second device operating at a second core frequency, the first core frequency being different that the second core frequency.

29. The method of claim 23, further comprising:

establishing a time unit quanta in the timing circuit compatible with a first device operating at first frequency and compatible with the first device operating at a second frequency.

30. A system, comprising:

a central processing unit;

a graphics device, the central processing unit coupled to the graphics device, the graphics device containing a graphics-rendering engine to concurrently render two or more independent images for display on multiple display devices, and

a time allocator to arbitrate the use of the graphics-rendering engine between the two or more independent images.

31. The system of claim 30, wherein the time allocator comprises:

a plurality of registers including a first register, the first register having a plurality of fields, a first field to determine whether the first register participates in an arbitration process to use the graphics rendering engine, a second field to point to a memory location containing instructions from a first instruction stream.

32. The system of claim 31, wherein the time allocator further comprises:

a first module to establish a programmable elapsed period of time to use the graphics-rendering engine.

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